CLAIMS

What is claimed is:

1. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers; and

managing movement of at least one of electrons and holes from said substrate towards said ONO layer by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

2. The method according to claim 1 wherein said managing comprises forming a thickness of said top oxide layer in a range of approximately 6-20 nm.

3. The method according to claim 1 wherein said managing comprises forming a thickness of said nitride layer in a range of approximately 1-2 nm.

4. The method according to claim 1 wherein said managing comprises forming a thickness of said bottom oxide layer in a range of approximately 4-5 nm.

5. The method according to claim 1 wherein said managing comprises forming said top oxide layer to be at least three times thicker than said nitride layer.

6. The method according to claim 1 wherein said managing comprises forming said top oxide layer to be approximately 3-20 times thicker than said nitride layer.

7. The method according to claim 1 wherein said managing comprises forming said top oxide layer to be at least 1.5 times thicker than said bottom oxide layer.

8. The method according to claim 1 wherein said managing comprises forming said top oxide layer to be approximately 1.5-4 times thicker than said bottom oxide layer.

9. The method according to claim 1 wherein said managing comprises forming said top oxide layer to be at least half of an overall thickness of said ONO layer.

10. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

decreasing a capacitance between said gate and said nitride layer by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

11. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

increasing a threshold voltage of said non-volatile memory device per number of electrons injectable into said nitride layer by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

12. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

decreasing a threshold voltage of said non-volatile memory device per number of holes injectable into said nitride layer by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

13. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

narrowing a distribution of electrons injectable into said nitride layer by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

14. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

improving a matching of electrons and holes injectable into said nitride layer by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

15. A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

enabling a reduction of operational current in said substrate by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

16. A method for operating a non-volatile memory device, the method comprising:

providing an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

applying operating voltages to said non-volatile memory device; and

controlling said operating voltages by controlling a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

17. A non-volatile memory device comprising:

a channel formed in a substrate;

two diffusion areas formed one on either side of said channel in said substrate, each diffusion area having a junction with said channel, said channel being adapted to permit movement of primary electrons to at least one of said diffusion areas; and

an oxide-nitride-oxide (ONO) layer formed at least over said channel, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

wherein a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer is adapted to manage movement of at least one of electrons and holes from said substrate towards said ONO layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

18. The device according to claim 17 wherein the thickness of said top oxide layer is approximately 6-20 nm.

19. The device according to claim 17 wherein the thickness of said nitride layer is approximately 1-2 nm.

20. The device according to claim 17 wherein the thickness of said bottom oxide layer is approximately 4-5 nm.

21. The device according to claim 17 wherein said top oxide layer is at least three times thicker than said nitride layer.

22. The device according to claim 17 wherein said top oxide layer is approximately 3-20 times thicker than said nitride layer.

23. The device according to claim 17 wherein said top oxide layer is approximately 1.5-4 times thicker than said bottom oxide layer.

24. The device according to claim 17 wherein said top oxide layer comprises at least half of an overall thickness of said ONO layer.